AFRL-SN-WP-TM-2005-1086

ROBUST, RELIABLE, RADIO FREQUENCY (RF) MICROELECTROMECHANICAL SYSTEMS (MEMS) CAPACITIVE SWITCHES

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JANUARY 2005

Interim Report for 23 August 2003 – 31 January 2005

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STINFO INTERIM REPORT

SENSORS DIRECTORATE
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WRIGHT-PATTERSON AIR FORCE BASE, OH 45433-7320

NOTICE

This technical report has been reviewed and is approved for publication.

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YY)*: January 2005

2. REPORT TYPE: Interim

3. DATES COVERED *(From - To)*: 08/23/2003 – 01/31/2005

4. TITLE AND SUBTITLE
ROBUST, RELIABLE, RADIO FREQUENCY (RF) MICROELECTROMECHANICAL SYSTEMS (MEMS) CAPACITIVE SWITCHES

5a. CONTRACT NUMBER: F33615-03-C-7003

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER: 69199F

6. AUTHOR(S)
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5d. PROJECT NUMBER: ARPS

5e. TASK NUMBER: ND

5f. WORK UNIT NUMBER: AN

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
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8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Sensors Directorate
Air Force Research Laboratory
Air Force Materiel Command
Wright-Patterson AFB, OH 45433-7320

10. SPONSORING/MONITORING AGENCY ACRONYM(S): AFRL/SNDD

11. SPONSORING/MONITORING AGENCY REPORT NUMBER(S): AFRL-SN-WP-TM-2005-1086

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

13. SUPPLEMENTARY NOTES
Report contains color.

This technical memo is a series of Microsoft PowerPoint slides.

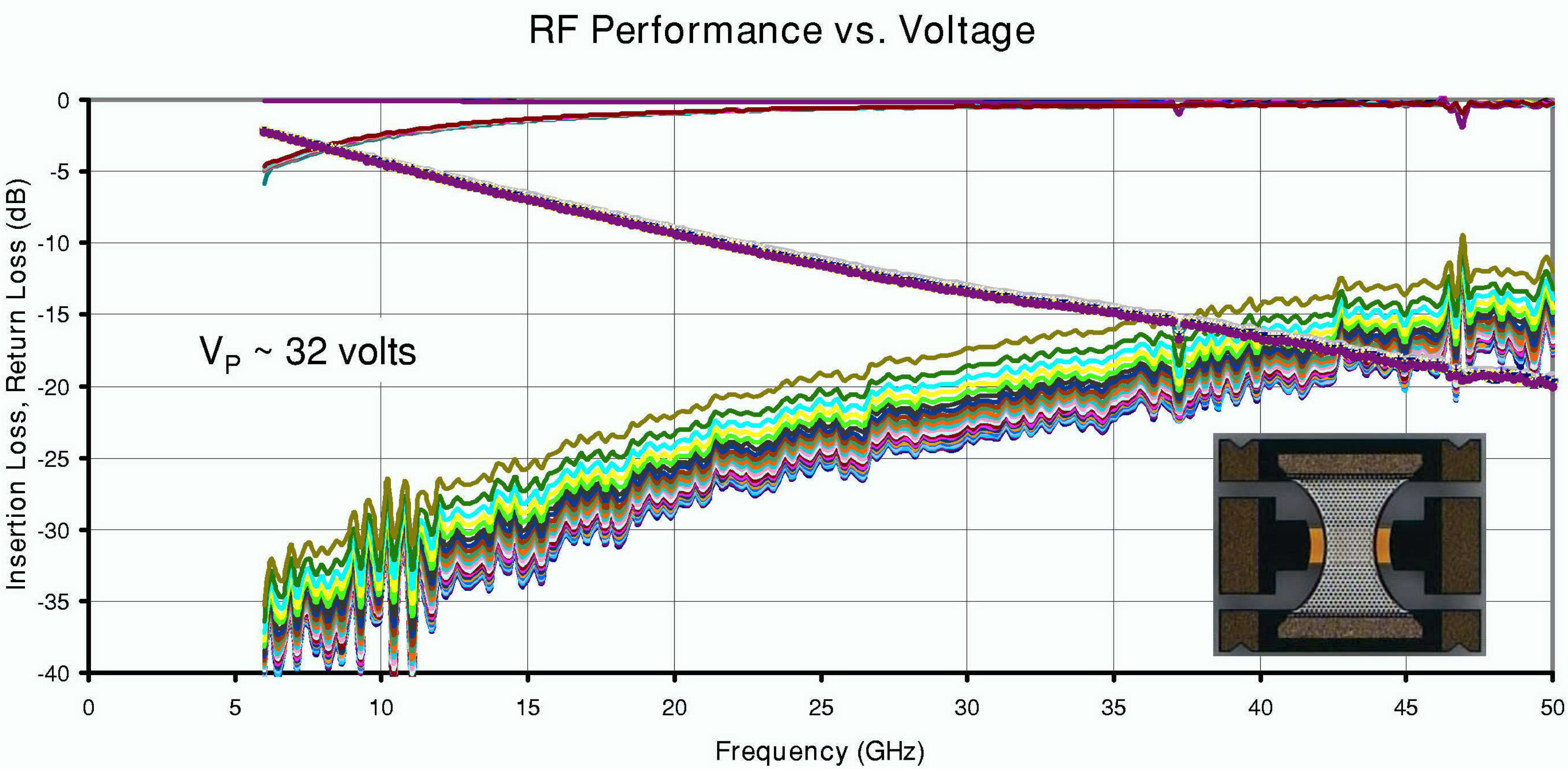
14. ABSTRACT
Wafer-level micro-encapsulation is an innovative, low-cost, wafer-level packaging method for encapsulating RF MEMS switches. This zero-level packaging technique has demonstrated < 0.1 dB package insertion loss up through 110 GHz and accounts for only 28 % of the total packaged RF MEMS circuit cost. This article overviews the processes, measurements, and testing methods used for determining the integrity and performance of individual encapsulated RF MEMS packages.

15. SUBJECT TERMS
Microelectromechanical Systems (MEMS), Radio Frequency (RF), Microwave Devices

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT:	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON (Monitor)
a. REPORT	b. ABSTRACT	c. THIS PAGE			John L. Ebel
Unclassified	Unclassified	Unclassified	SAR	20	19b. TELEPHONE NUMBER *(Include Area Code)* (937) 255-1874 x3462

Standard Form 298 (Rev. 8-98)
Prescribed by ANSI Std. Z39-18

RF Switch Characterization



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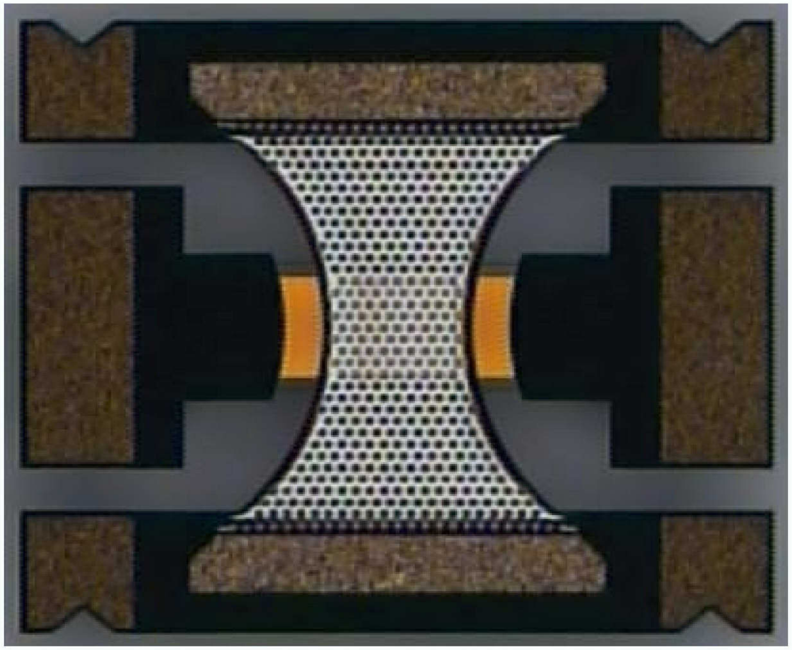
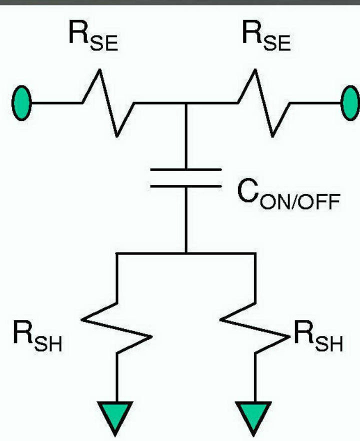
RF Capacitive Switch Model





Summary

Insertion Loss @ 35 GHz	~0.06	dB
Isolation @ 35 GHz	15	dB

Model Values

Rse	0.18	Ohms
Rsh	0.24	Ohms
Coff	0.015	pF
Con	0.73	pF
Ron	0.25	Ohms
Capacitance Ratio	50	
Cutoff Frequency	>2,000	GHz
Switching Speed	< 40	µs
Intercept Point	TBD	dBm
Switching Voltage	25-35	volts

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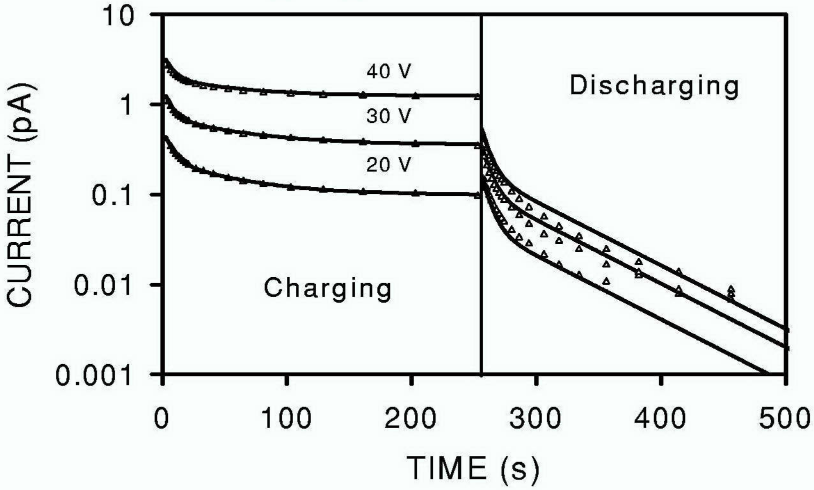
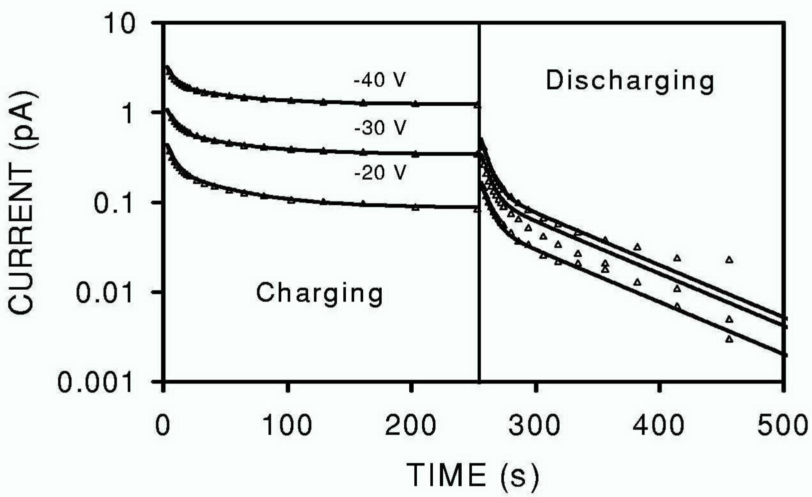
Dielectric Charging Characterization

Charging Characterization

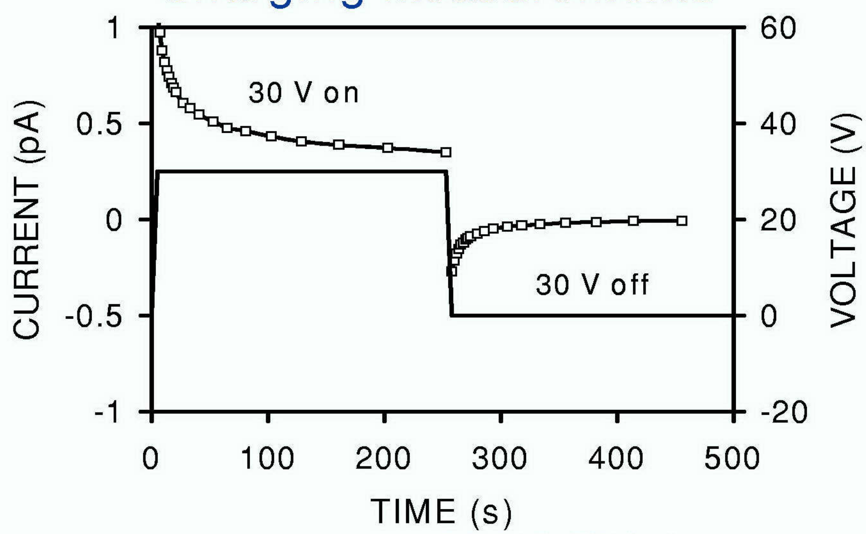




Dielectric Charging Characterization

- Uses transient current spectroscopy to measure charging and discharging of carriers within capacitor dielectrics
- Requires measurement of very small currents, ~femtoamps
- Use measurements to extract carrier densities and time constants as a function of applied voltage

Charging Measurements



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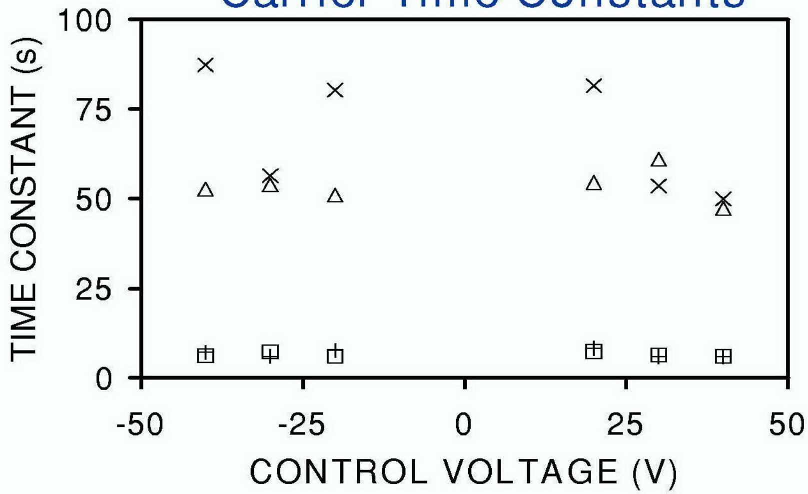
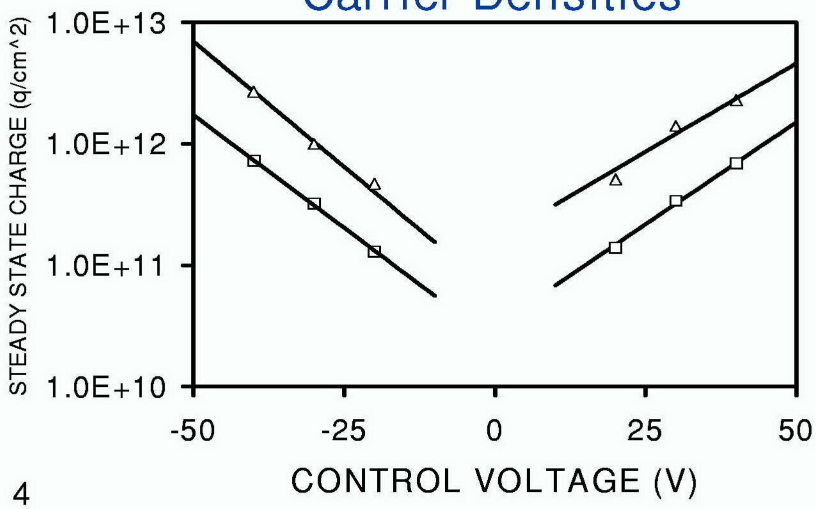
Modeling of Dielectric Charging

Carrier Time Constants



Carrier Densities



Charging Model

$$\Delta Q = \sum_{J} \Delta Q_0^J(V)\left[1 - \exp(-t_{ON}/\tau_C^J)\right]\exp(-t_{OFF}/\tau_D^J)$$

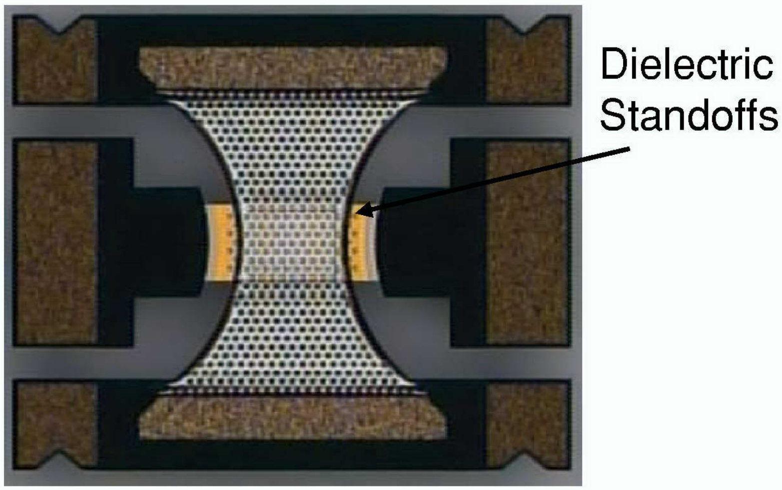
Extracted Model Parameters

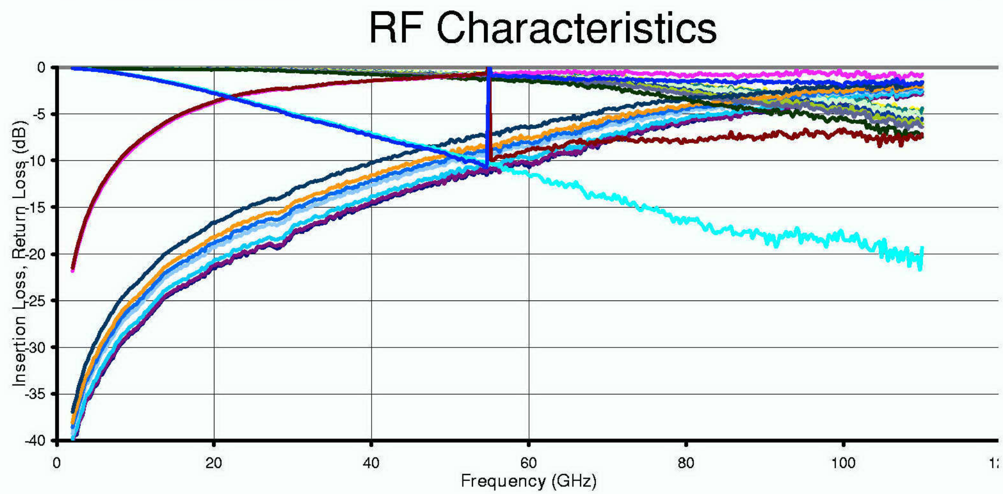
POSITIVE BIAS				
J	t_C (s)	t_D (s)	Q_0 (cm^{-2})	V_0 (V)
1	6.6	6.8	3.1×10^{10}	12.9
2	54.3	61.6	1.6×10^{11}	14.9
NEGATIVE BIAS				
J	t_C (s)	t_D (s)	Q_0 (cm^{-2})	V_0 (V)
1	6.5	7.0	2.4×10^{10}	11.7
2	52.5	74.7	6.0×10^{10}	10.5

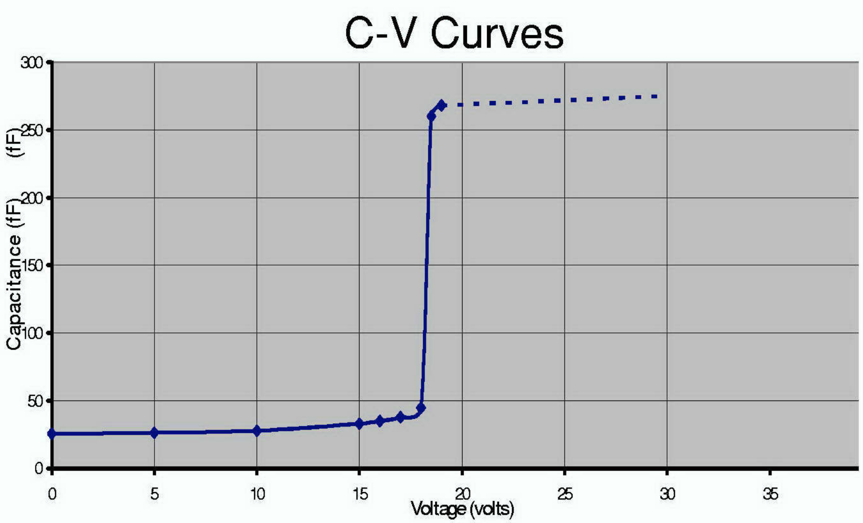
Results

- Measurements demonstrate two carrier types contributing to charging
- One has a short time constant, 6-7s, and the other long, 50-75s.
- Exponential dependence on control voltage

Proximity Switch







- Initial design shows good capacitance ratio (~ 10:1)
- Very low insertion loss
- Switches tend to burn out due to shorting of the membrane and electrode
- Characterization ongoing at a low level

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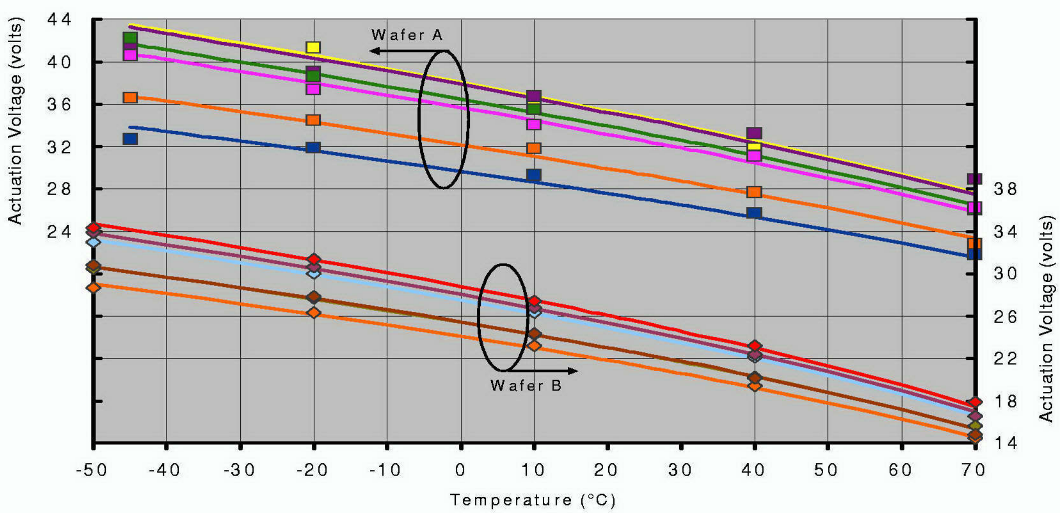
Reducing Variation in Actuation Voltage

$$V_P(T) = \sqrt{\frac{64\,\gamma_g (1-\nu) t g_o^3}{27\,L^2 \varepsilon_o} \left(\Delta \alpha E (T_{zs} - T)\right)}$$



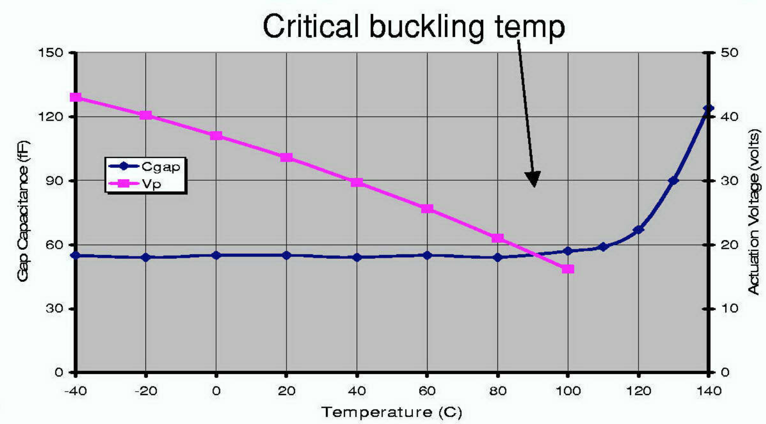
Wafer A Tzs 148.01 Deg C

Device	1	2	3	4	5	6
Gap (□m)	1.92	2.27	2.26	2.21	2.03	2.18

Wafer B Tzs 110.41 Deg C

Device	1	2	3	4	5	6
Gap (□m)	2.02	2.04	2.08	1.91	1.85	1.92

Membrane gap constant over temp



- Prior publications showed 36 volts to 60 volts variation over -50°C to +70°C
- Assumed linear relationship
- This project demonstrated 21 volts to 22 volts variation over temperature
- Demonstrated correlation between theory and measured data to square-root relationship

RF MEMS Micro-Encapsulation

Patent Pending

Micro-Encapsulation Process Flow

Process:

Prior to membrane release, add a second sacrificial layer on top of switch.

Deposit/pattern/etch an insulating cage structure on top of sac layer.

Release both sacrificial layers.

Apply spin-on glass to encapsulate switches (surface tension restricts flow of encapsulant).

Advantages (beyond wafer-level pkg):

- Lower temperature processing.
- No wafer bonding or alignment required.
- No significant packaging loss or parasitics!
- No separate seal ring or interconnect area required, ~85% more die for a 4 x 6 mm IC.
- No expensive thru-wafer vias required.
- CMOS compatible, an excellent way to seal RF MEMS co-integrated with GaAs or SiGe MMICs.
- Package cost ~30% of total die cost.

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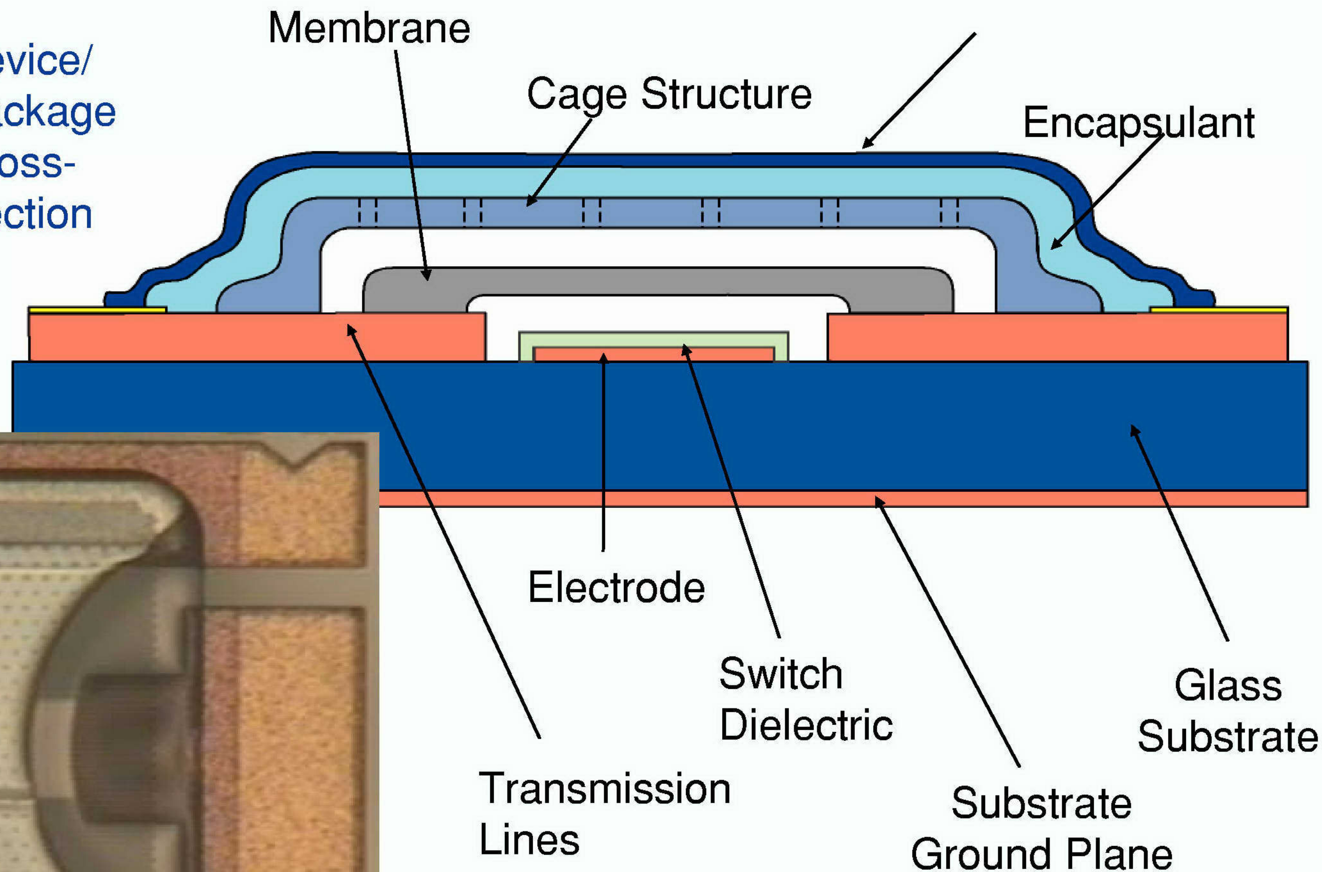
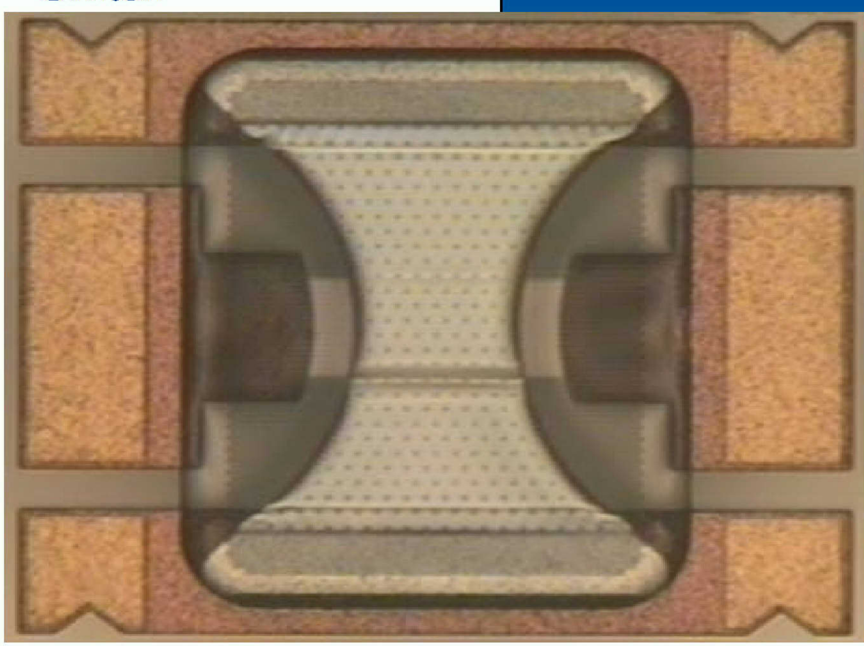
Wafer-Level Microencapsulation

“Nanoliter Packaging”

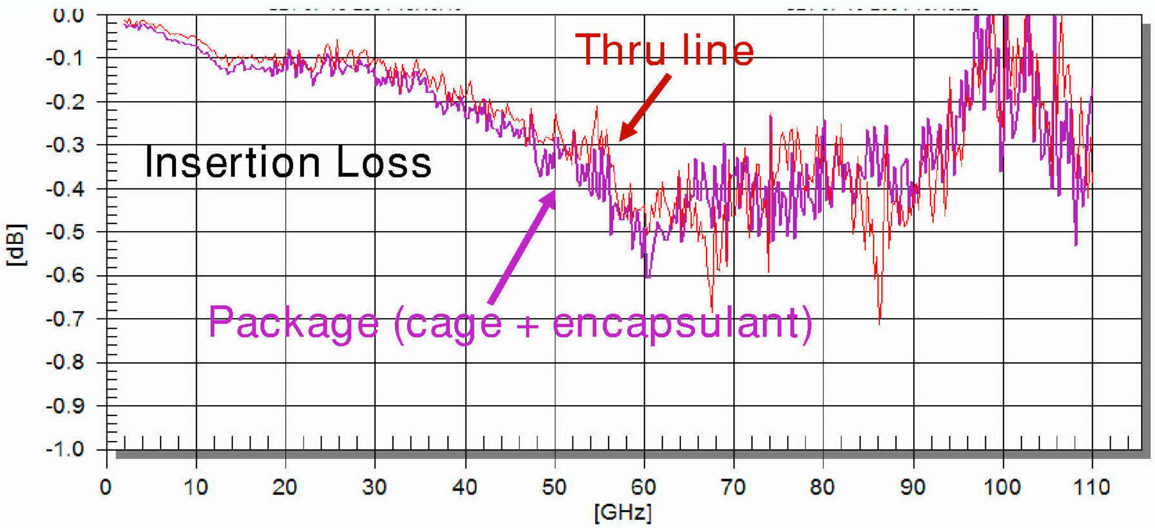
Device/ Package Cross-Section

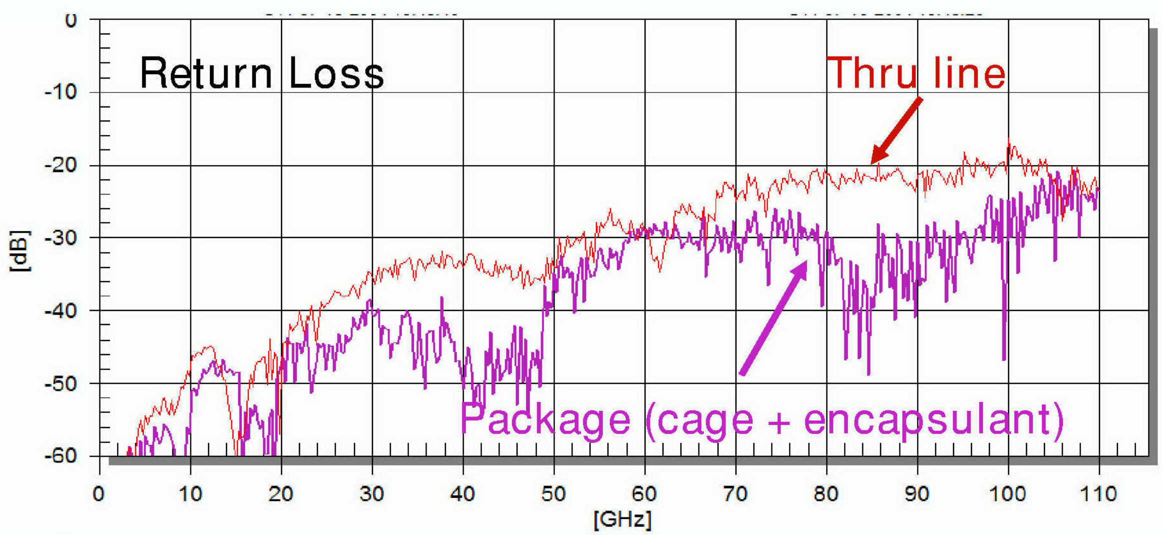


Packaged Capacitive Switch



Packages work to 110 GHz+!!





- Packages exhibit excellent <u>measured</u> performance to 110 GHz !
- Full package loss < 0.1 dB to 110 GHz with > 20 dB return loss
- Losses very difficult to measure as they are on same order as measurement uncertainty

Thanks to Prof. Papapolymerou and student Matt Morton

Georgia Tech

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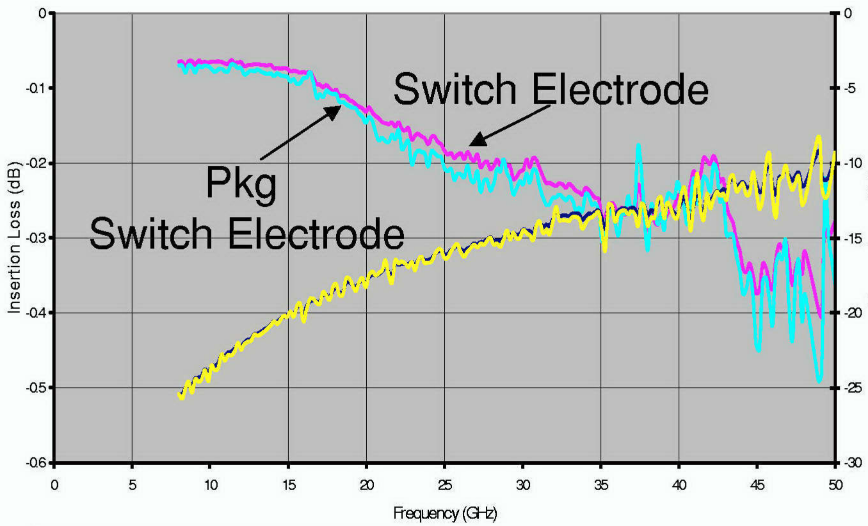
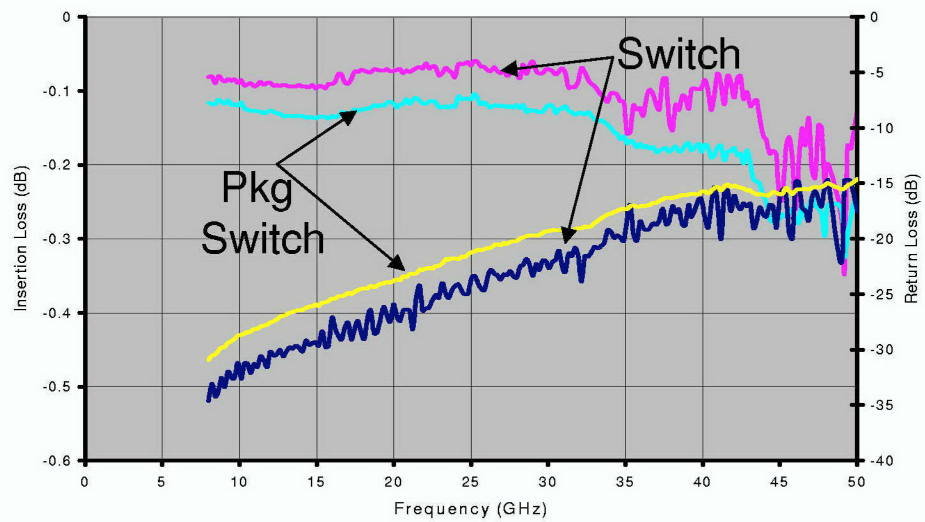
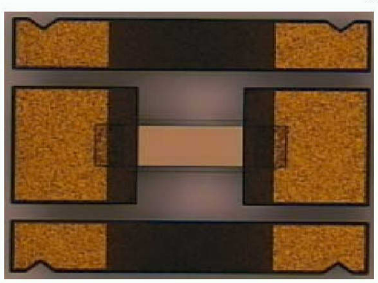
RF Loss Comparisons – Packaged Structures

Packaged Switch Electrode

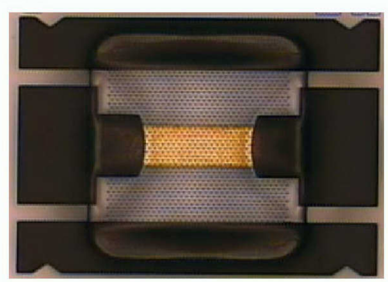


Packaged Switch

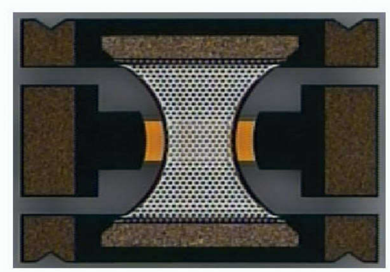




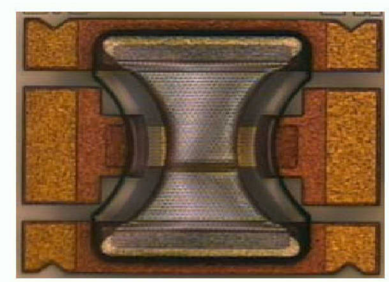
Switch Electrode



Packaged Switch Electrode



Switch



Packaged Switch

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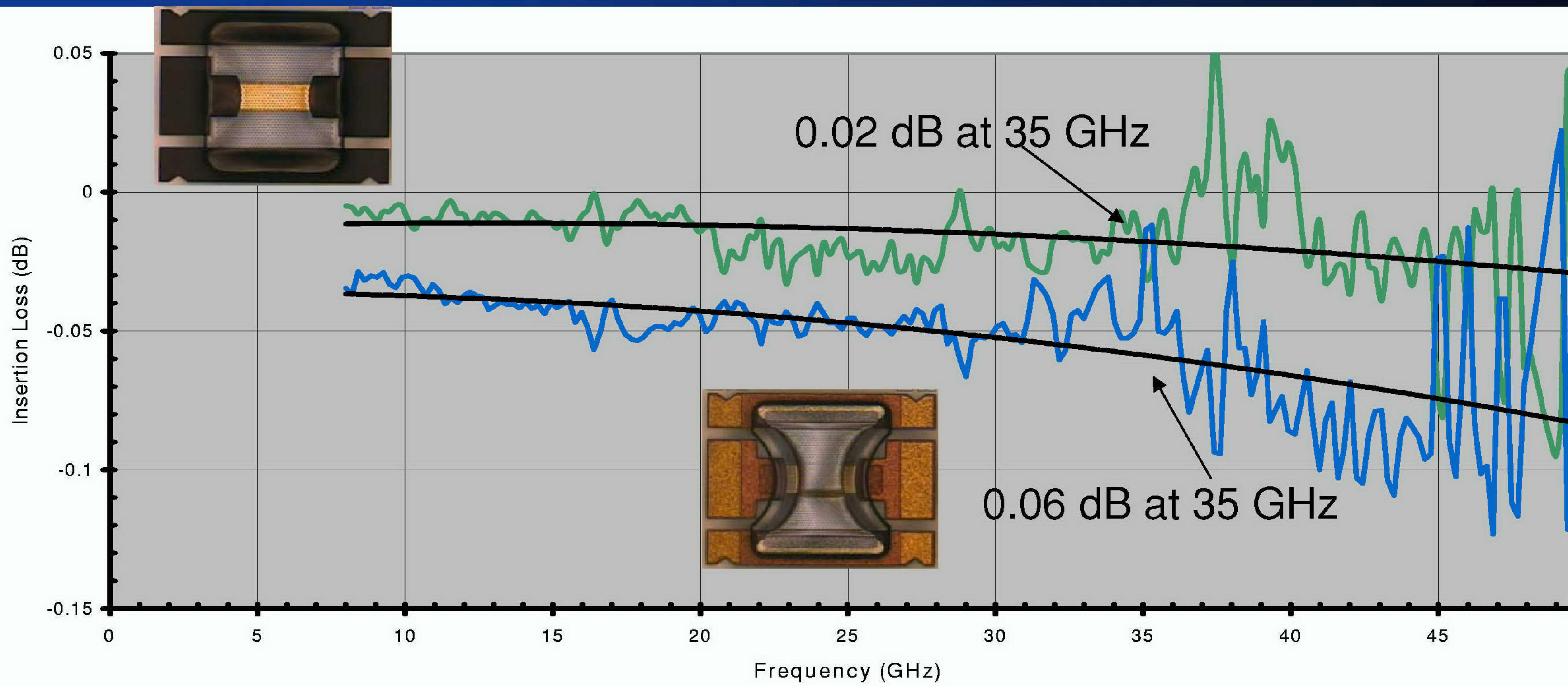
Total Package Loss



Results of Packaging Comparisons

- Excellent performance measured through 110 GHz with < 0.1 dB loss
- No significant degradation in return loss
- Absolutely no package resonances
- Package loss is approximately 0.02-0.06 dB at 35 GHz

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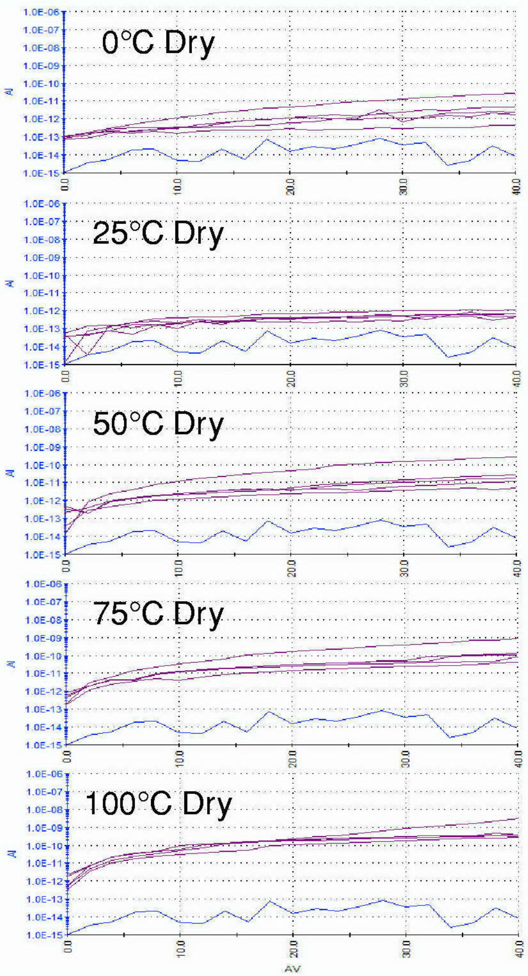
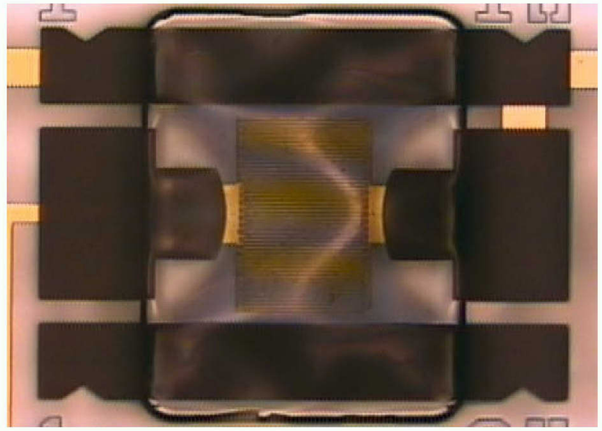
Package Humiticity Sensors



Sensor Calibration Data

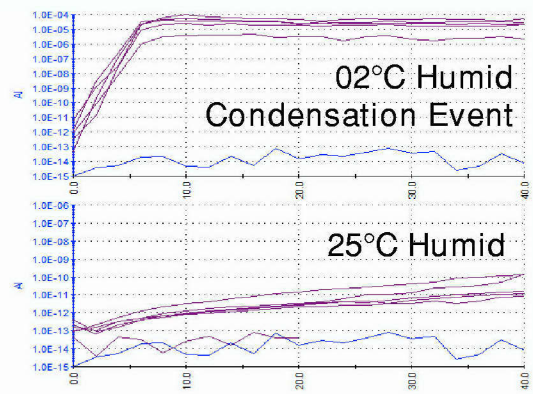


Microencapsulated Dew Point Sensor

- Humiditicity sensor consists of interdigitated capacitor with 2.5μm lines/spaces
- Fits into same area/ volume as MEMS switch
- Measures surface conductivity due to adsorbed moisture

Failure Criteria

- Failure criteria taken to be equivalent moisture of 25°C at 30-50% humidity
- Moisture has sufficient surface adhesion to imped operation of a membrane switch
- Failure level ~50 10^{-12} amps



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Microencapsulation Humiticity Measurements

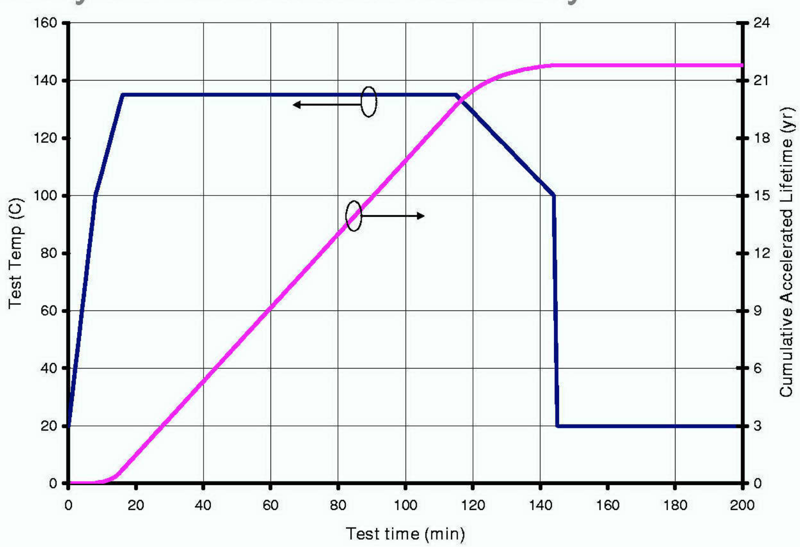
Procedure

- Select 12 packaged sensors for accelerated testing
- Subject packages to accelerated test sequences of 130°C/100% humidity for 1.5 hours
- Characterize sensor I-V curve to determine adsorbed moisture

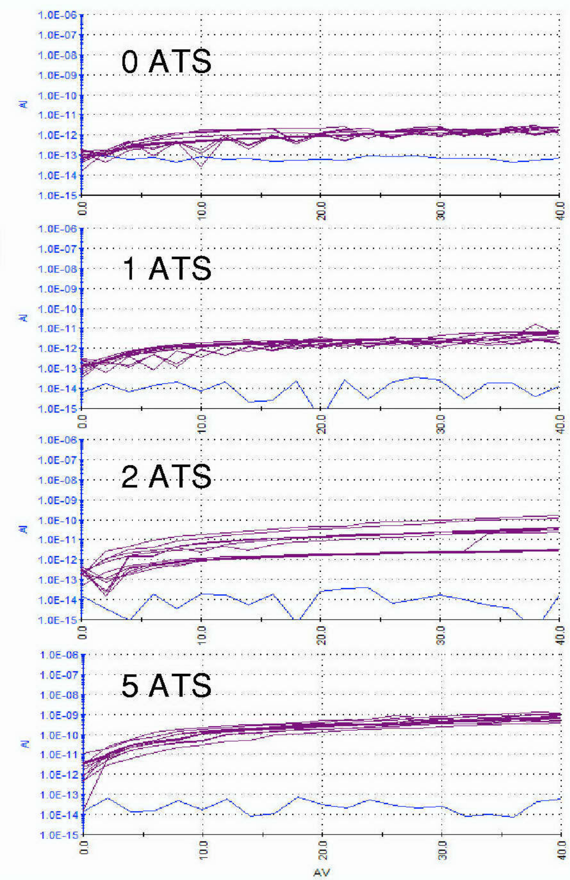
Results

- Initial encapsulation layer withstands 2 ATSs before defined failure level is reached
- This is equivalent to 42 years at 25°C/50% humidity or 2 years of jungle conditions at 35°C/85% humidity
- Additional sealant layers will increase humiticity

Humidity/ Temperature Accelerated Test Sequence (ATS)



Accelerated Humiticity Results



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